Advanced High-K Gate Dielectric for High-Performance Short-Channel $In_{0.7}Ga_{0.3}As$ Quantum Well Field Effect Transistors on Silicon Substrate for Low Power Logic Applications

M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau*, J. Kavalieros, W. K. Liu*, D. Lubyshev*, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and Robert Chau

Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

* IQE Inc, Bethlehem, PA 18015, USA

Contact: robert.s.chau@intel.com

Abstract

This paper describes integration of an advanced composite high-K gate stack (4nm $TaSiO_x$-2nm InP) in the $In_{0.7}Ga_{0.3}As$ quantum-well field effect transistor (QWFET) on silicon substrate. The composite high-K gate stack enables both (i) thin electrical oxide thickness (t_{OXE}) and low gate leakage (J_G) and (ii) effective carrier confinement and high effective carrier velocity (V_{eff}) in the QW channel. The L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with this composite high-K gate stack achieves high transconductance of 1750μS/μm and high drive current of 0.49mA/μm at V_{DS}=0.5V.

Introduction

$In_{0.7}Ga_{0.3}As$ QWFET is a promising transistor candidate for future high-speed low-power logic applications due to its excellent drive current performance at low voltage, and its demonstrated integration onto the silicon substrate [1]. However at present the InGaAs QWFET uses a Schottky gate with no gate dielectric and is subjected to large gate leakage (J_G) with scaling of the upper InAlAs barrier thickness above the quantum well (QW) (Fig. 1). For further transistor scaling, there are significant challenges in identifying a suitable high dielectric constant (K) gate dielectric and its integration into the III-V transistor, which will need to simultaneously decrease t_{OXE} (electrical gate oxide thickness), reduce J_G, achieve good interface properties while retaining high carrier mobility in the transistor channel. In this work, we demonstrate a composite high-K $TaSiO_x$-InP gate stack and its integration into the $In_{0.7}Ga_{0.3}As$ QWFET, resulting in high-performance short-channel $In_{0.7}Ga_{0.3}As$ QWFETs on silicon substrate with significantly decreased t_{OXE} and reduced J_G.

Materials Growth and Characterization

In order to retain the high carrier mobility of the QWFET, the high-K gate dielectric is deposited on the upper barrier of the QW stack rather than directly on the $In_{0.7}Ga_{0.3}As$ QW channel. Two upper barrier materials, $In_{0.52}Al_{0.48}As$ and InP, with identical lattice constants and similar K-values are evaluated for high-K gate dielectric integration. Figs. 2a-b show the gate capacitance (C) versus gate bias (V_G) for Al_2O_3 capacitors on $In_{0.52}Al_{0.48}As$ and InP respectively. Al_2O_3-InP capacitors exhibit lower frequency dispersion than Al_2O_3-$In_{0.52}Al_{0.48}As$ capacitors, suggesting InP is a more suitable upper barrier material for high-K integration. Further improvements can be made to the high-K-InP capacitors by replacing Al_2O_3 with $TaSiO_x$ which has higher K and similar frequency dispersion, as shown in Fig. 3.

Fig. 4 shows a schematic of the new $In_{0.7}Ga_{0.3}As$ QWFET for this work with 2nm InP upper barrier layer and a 4nm $TaSiO_x$ high-K gate dielectric, which form a composite $TaSiO_x$-InP gate stack on top of the QW. The thickness of these layers is chosen to provide a thin t_{OXE} while maintaining carrier confinement in the QW. Fig. 5 shows the band diagram of the $In_{0.7}Ga_{0.3}As$ QW structure with 2nm InP upper barrier obtained using Schrödinger-Poisson simulation, which indicates good carrier confinement in the $In_{0.7}Ga_{0.3}As$ QW layer. Figs. 6a-b show the TEM micrographs of the entire $In_{0.7}Ga_{0.3}As$ QWFET stack on silicon by MBE and the active device layers with 2nm InP upper barrier, respectively. The effectiveness of the 2nm InP layer as an upper barrier is confirmed in Fig. 7 which shows QW electron mobility of 10,000 cm^2/Vs at 300K with no parallel conduction.

Device Fabrication and Characterization

The TEM in Fig. 8 shows the $In_{0.7}Ga_{0.3}As$ QWFET with physical gate length (L_G) of 75nm and the composite 4nm $TaSiO_x$-2nm InP gate stack. The high-K $TaSiO_x$ dielectric was deposited using ALD, and the metal gate electrode consists of TiN/Pt/Au. Fig. 9a shows the C-V_G measured on the $In_{0.7}Ga_{0.3}As$ QWFET with the composite $TaSiO_x$-InP gate stack. The composite gate stack has t_{OXE} of 22Å determined from the measured intrinsic gate capacitance, and also good stability with minimal C-V_G hysteresis. Included is C-V_G of the Schottky-gate QWFET (extracted at RF due to high J_G) with t_{InAlAs}=5nm and t_{OXE}=33Å. Fig. 9b shows J_G as a function of V_G for the $In_{0.7}Ga_{0.3}As$ QWFET with (i) composite $TaSiO_x$-InP gate stack versus (ii) Schottky gate. Insertion of high-K gate dielectric into the $In_{0.7}Ga_{0.3}As$ QWFET decreases t_{OXE} by 11Å while simultaneously reducing the gate leakage by a factor of >1000.

Fig. 10 shows drain current (I_D) versus gate voltage (V_{GS}) of L_G=180nm $In_{0.7}Ga_{0.3}As$ QWFET with the composite $TaSiO_x$-InP gate stack. The device shows both excellent subthreshold slope (SS) of 85mV/decade and drain induced

barrier lowering (DIBL) of 35mV/V at V_{DS}=0.5V. Figs. 11-12 show the I_D-V_{GS} and the I_D-V_{DS} characteristics respectively of the L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET with the composite gate stack. The drive current and peak transconductance (G_m) of this L_G=75nm device are 0.49mA/μm and 1750μS/μm (Fig. 13) respectively at low V_{DS} of 0.5V. These performance values are the highest ever reported for III-V QWFET with high-K gate dielectric. Fig. 14 shows the measured effective electron velocity (V_{eff}) in the $In_{0.7}Ga_{0.3}As$ QWFETs with composite $TaSiO_x$-InP gate stack is >3.5X higher than that in strained Si MOSFETs [2]. This demonstrates that despite the insertion of a composite high-K gate stack, the intrinsic advantage of $In_{0.7}Ga_{0.3}As$ QWFET over strained Si MOSFET is still maintained. Figs. 15-16 show the G_m and SS respectively as a function of L_G for the $In_{0.7}Ga_{0.3}As$ QWFETs with composite gate stack versus those of the state-of-the-art III-V transistors with high-K gate dielectrics reported in literature [3-6]. The data shows the transistors of this work have significantly improved SS and higher G_m for all L_G due to thinner t_{OXE} and better high-K gate stack properties.

Conclusions

An advanced composite high-K gate stack (4nm $TaSiO_x$-2nm InP) has been integrated in the $In_{0.7}Ga_{0.3}As$ QWFET on silicon substrate to enable both (i) thin t_{OXE} and low J_G and (ii) effective carrier confinement and high V_{eff} in the QW channel. The L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET with this composite high-K gate stack achieves high G_m of 1750μS/μm and high drive current of 0.49mA/μm at V_{DS}=0.5V, and also >3.5X improvement in V_{eff} over strained Si MOSFETs at the same DIBL. Compared to the state-of-the-art III-V transistors with high-K gate dielectrics reported in literature, this work shows significantly improved SS and higher G_m for all L_G due to thinner t_{OXE} and better high-K gate stack properties.

References

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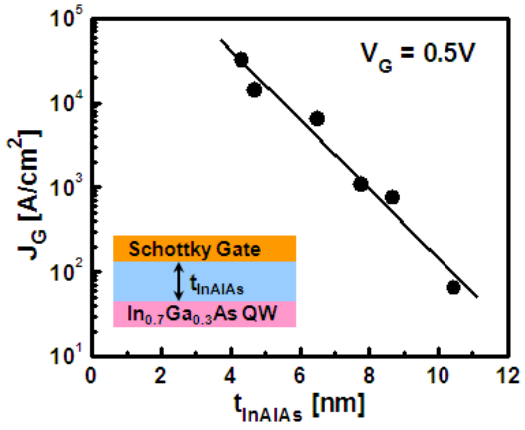

Fig. 1: Gate leakage current (J_G) versus $In_{0.52}Al_{0.48}As$ barrier thickness (t_{InAlAs}) between the metal gate electrode and $In_{0.7}Ga_{0.3}As$ QW. High J_G is due to thin t_{InAlAs} and the low band offset between the barrier and the channel.

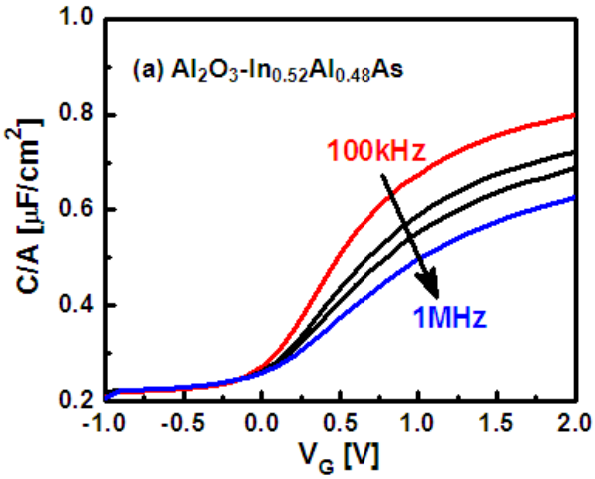

Fig. 2(a): Gate capacitance (C) versus gate bias (V_G) for Al_2O_3-$In_{0.52}Al_{0.48}As$ capacitors as a function of measurement frequency.

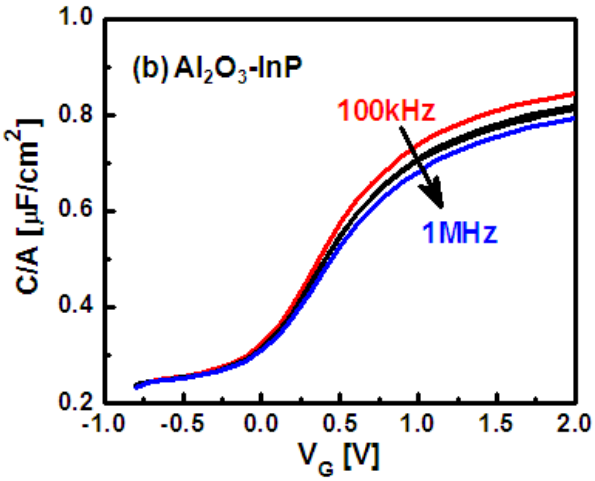

Fig. 2(b): Gate capacitance (C) versus gate bias (V_G) for Al_2O_3-InP capacitors as a function of measurement frequency. Al_2O_3-InP capacitors exhibit lower frequency dispersion (7%/decade) than Al_2O_3-$In_{0.52}Al_{0.48}As$ capacitors (27%/decade), indicating InP is a more suitable material for high-K integration.

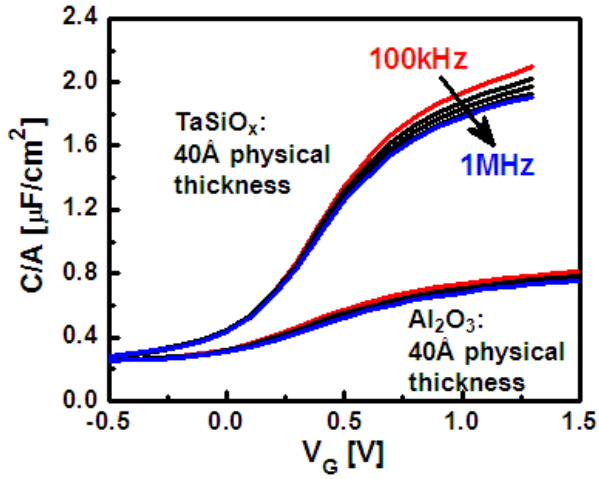

Fig. 3: Gate capacitance (C) versus gate bias (V_G) for 40Å $TaSiO_x$ and 40Å Al_2O_3 dielectrics on InP. $TaSiO_x$ shows higher gate capacitance than Al_2O_3 due to its higher dielectric constant. Both systems show similar frequency dispersion (7%/decade).

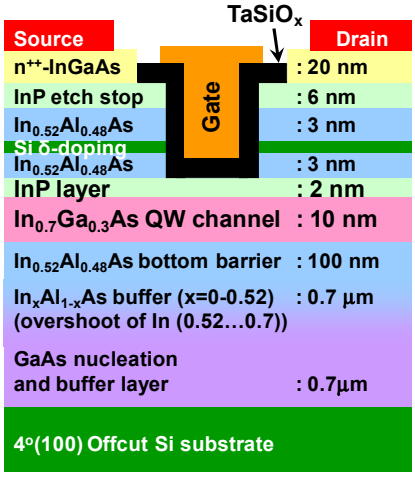

Fig. 4: Schematic of $In_{0.7}Ga_{0.3}As$ QWFET on silicon with 2nm InP upper barrier layer and a 4nm $TaSiO_x$ high-K gate dielectric, which form a composite $TaSiO_x$-InP gate stack.

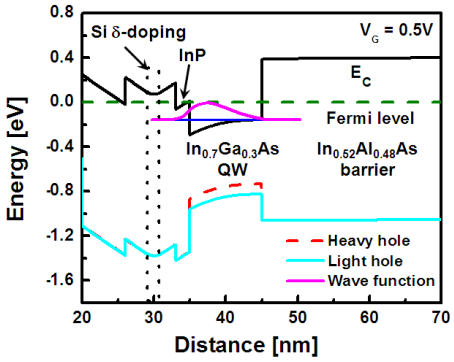

Fig. 5: Band diagram of $In_{0.7}Ga_{0.3}As$ QW stack with 2nm InP top barrier obtained using Schrödinger-Poisson simulation, indicating carrier wave-function confinement in the $In_{0.7}Ga_{0.3}As$ QW. Conduction band (E_C), heavy and light hole bands and Fermi level are shown.

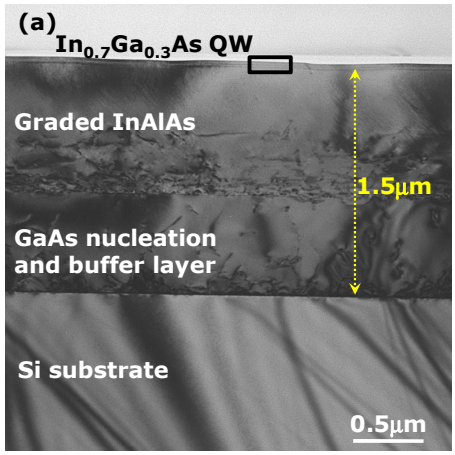

Fig. 6(a): Cross-sectional TEM micrograph of $In_{0.7}Ga_{0.3}As$ QW stack with InP top barrier layer on Si substrate via 1.5µm composite buffer. All III-V layers were grown using MBE.

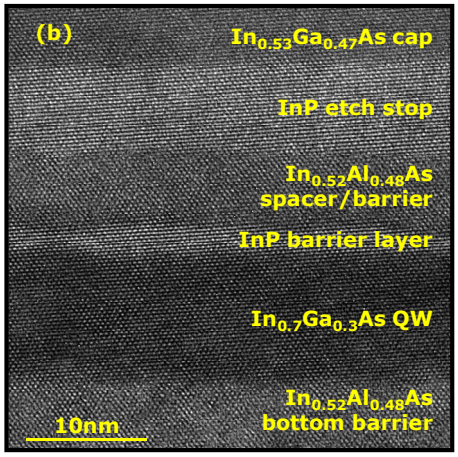

Fig. 6(b): High-resolution TEM micrograph of $In_{0.7}Ga_{0.3}As$ QW stack with 2nm InP top barrier layer. All III-V layers were grown using MBE.

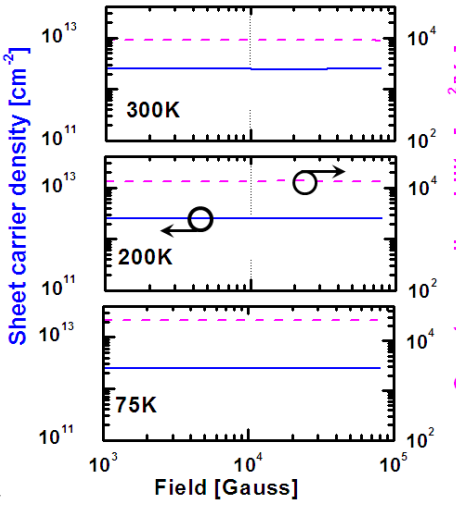

Fig. 7: Sheet carrier density and electron mobility versus magnetic field of $In_{0.7}Ga_{0.3}As$ QW stack with InP top barrier layer at different temperatures, showing no parallel conduction. The mobility in the $In_{0.7}Ga_{0.3}As$ QW is 10,000 cm^2/Vs at 300K.

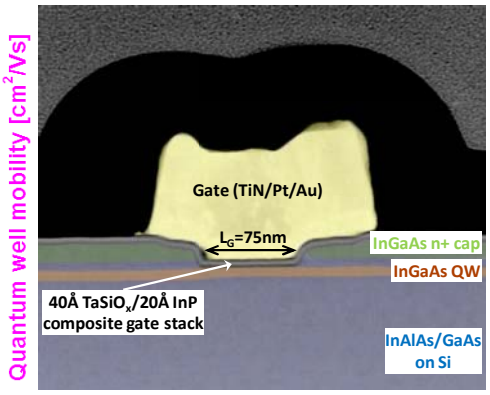

Fig. 8: TEM micrograph of the L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET showing the 2nm InP upper barrier layer and 4nm ALD-deposited $TaSiO_x$ high-K gate dielectric, which form a composite $TaSiO_x$-InP gate stack. The metal gate electrode consists of TiN/Pt/Au.

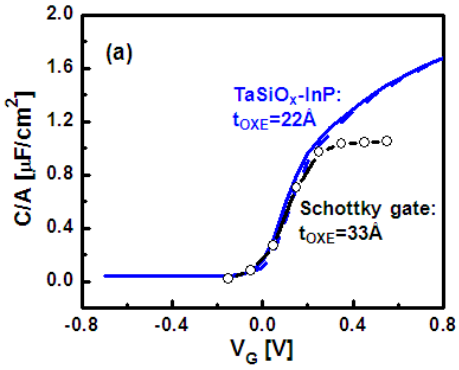

Fig. 9(a): C-V_G measured on the $In_{0.7}Ga_{0.3}As$ QWFET with the composite 4nm $TaSiO_x$-2nm InP gate stack showing minimal hysteresis and t_{OXE}=22Å. Included is C-V_G of the Schottky-gate QWFET (extracted at RF due to high J_G) with t_{InAlAs}=5nm and t_{OXE}=33Å.

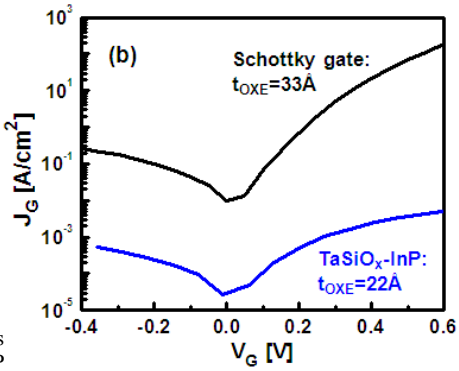

Fig. 9(b): J_G versus V_G of $In_{0.7}Ga_{0.3}As$ QWFET with the same (i) composite gate stack and (ii) Schottky gate electrode as Fig. 9(a).

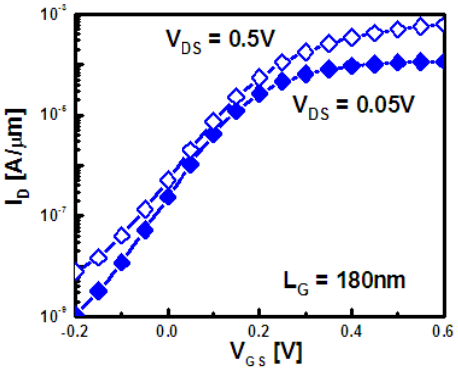

Fig. 10: Drain current (I_D) versus gate voltage (V_{GS}) of L_G=180nm $In_{0.7}Ga_{0.3}As$ QWFET with composite 4nm $TaSiO_x$-2nm InP gate stack (t_{OXE}=22Å). At V_{DS}= 0.5V the device shows excellent subthreshold slope (SS) =85mV/dec and drain induced barrier lowering (DIBL) =35mV/V.

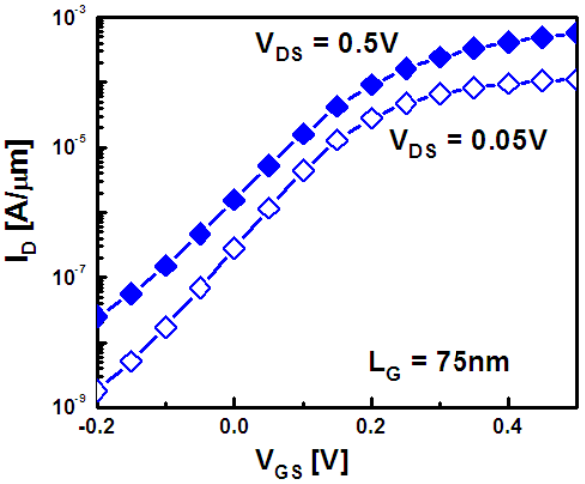

Fig. 11: Drain current (I_D) versus gate voltage (V_{GS}) of L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET with composite 4nm $TaSiO_x$-2nm InP gate stack (t_{OXE}=22Å). At V_{DS}= 0.5V the device shows drive current of 0.49mA/μm over 0.5V V_{GS} swing.

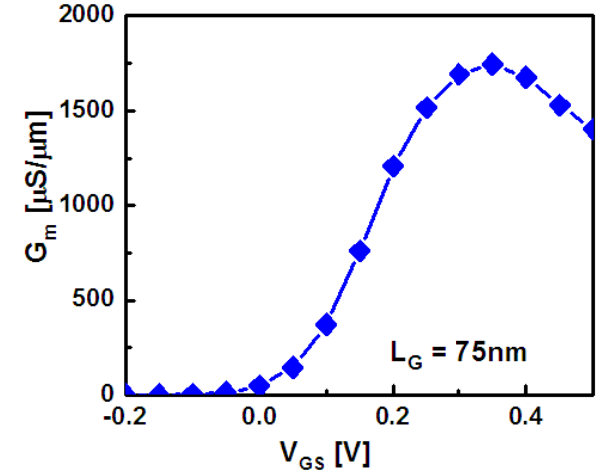

Fig. 13: Transconductance (G_m) characteristics of L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET with composite 4nm $TaSiO_x$-2nm InP gate stack (t_{OXE}=22Å). Peak G_m is 1750μS/μm at V_{DS}= 0.5V, which is highest ever reported for III-V QWFET with high-K dielectric.

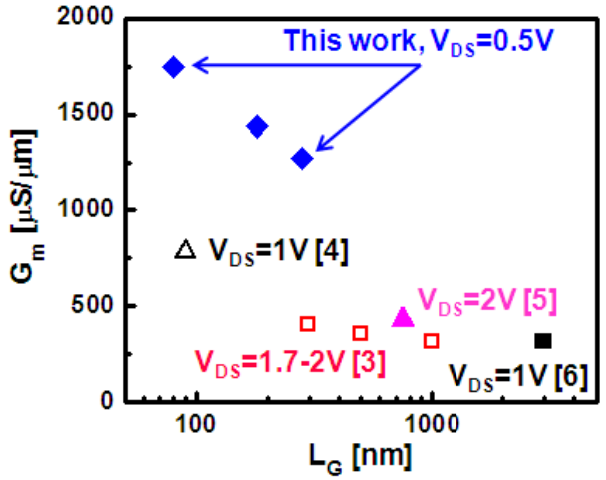

Fig. 15: Peak transconductance (G_m) as a function of gate length (L_G) for the $In_{0.7}Ga_{0.3}As$ QWFETs with composite gate stack of this work versus that of the state-of-the-art III-V transistors with high-K gate dielectrics reported in literature [3-6].

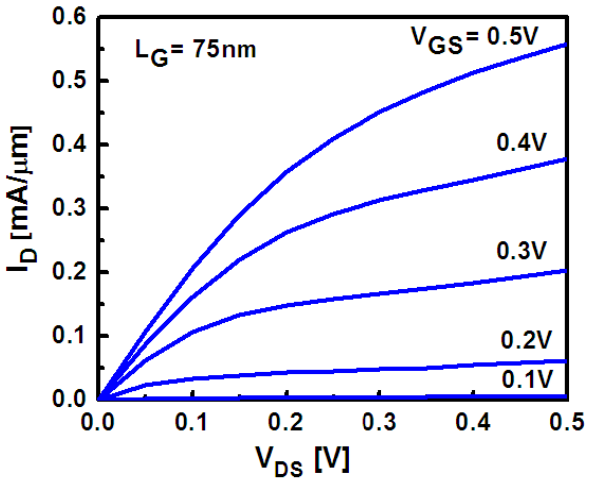

Fig. 12: I_D-V_{DS} of L_G=75nm $In_{0.7}Ga_{0.3}As$ QWFET with composite 4nm $TaSiO_x$-2nm InP gate stack (t_{OXE}=22Å).

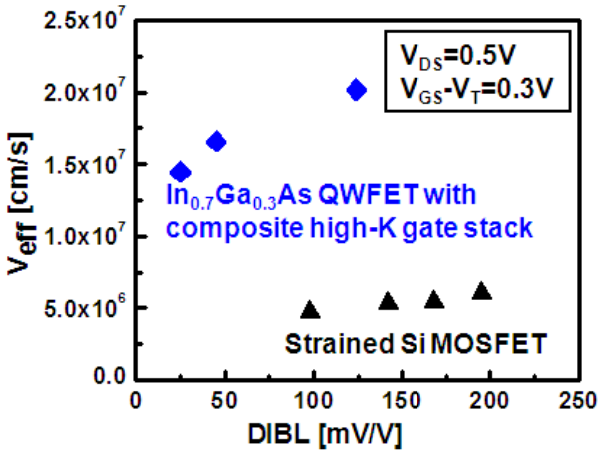

Fig. 14: Measured effective electron velocity (V_{eff}) versus DIBL comparing $In_{0.7}Ga_{0.3}As$ QWFET with composite 4nm $TaSiO_x$-2nm InP gate stack (t_{OXE}=22Å) and strained Si MOSFET at V_{DS}=0.5 V and gate overdrive of (V_{GS}−V_T)=0.3V. InGaAs QWFET with high-K gate dielectric shows more than 3.5X increase in V_{eff} over strained Si.

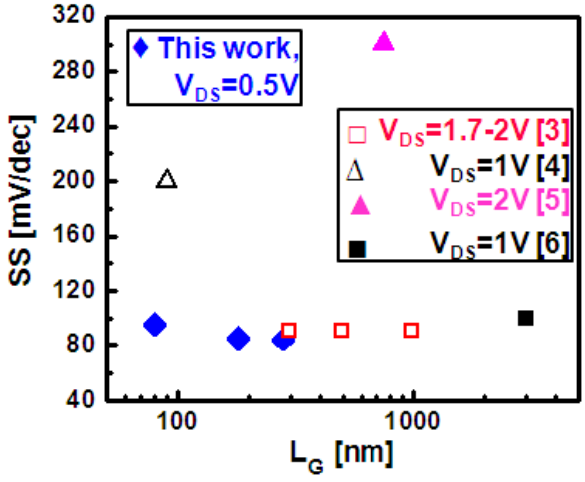

Fig. 16: Subthreshold slope (SS) as a function of gate length (L_G) for the $In_{0.7}Ga_{0.3}As$ QWFETs with composite gate stack of this work versus that of the state-of-the-art III-V transistors with high-K gate dielectrics reported in literature [3-6].